Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	147	HDP with (ICP or (inductively adj coupled adj plasma))	US-PGPUB; USPAT	OR	ON	2005/11/03 16:35
L8	131	6 and oxide and (silicon or zinic)	US-PGPUB; USPAT	OR	ON	2005/11/03 16:36
L9	117	8 and @ad<"20040315"	US-PGPUB; USPAT	OR	ON	2005/11/03 16:44
L10	117	9 and (wafer or (work adj piece) or object or substrate)	US-PGPUB; USPAT	OR	ON	2005/11/03 16:38
L11	10	10 and (treat or treating)	US-PGPUB; USPAT	OR	ON	2005/11/03 16:43
L12	153	((treat or treating) with (ICP or (inductively adj coupled adj plasma)))	US-PGPUB; USPAT	OR	ON	2005/11/03 16:46
L13	5	12 and ((forming or depositing) with oxide)	US-PGPUB; USPAT	OR	ON	2005/11/03 16:47
L14	3	13 and @ad<"20040315"	US-PGPUB; USPAT	OR	ON	2005/11/03 17:14
L15	22	((treat or treating) with (ICP or (inductively adj coupled adj plasma)))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/03 16:46
L16	0	15 and ((forming or depositing) with oxide)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/03 16:47
L17	145	12 and @ad<"20040315"	US-PGPUB; USPAT	OR	ON	2005/11/03 16:47
L18	105	17 and (oxide or dioxide)	US-PGPUB; USPAT	OR	ON	2005/11/03 16:47
L19	0	(high adj density adj inductively adj plasma) and @ad<"20040315"	US-PGPUB; USPAT	OR	ON	2005/11/03 17:15
L20	1113	((high adj density) with inductively) and @ad<"20040315"	US-PGPUB; USPAT	OR	ON	2005/11/03 17:15
L21	1101	((high adj density) with inductively with plasma) and @ad<"20040315"	US-PGPUB; USPAT	OR	ON	2005/11/03 17:15
L22	510	((high adj density) near3 inductively near3 plasma) and @ad<"20040315"	US-PGPUB; USPAT	OR	ON	2005/11/03 17:16
L24	505	22 and (substrate or wafer)	US-PGPUB; USPAT	OR	ON	2005/11/03 17:16
L25	11	22 and ((treat or treating) with (substrate or wafer))	US-PGPUB; USPAT	OR	ON	2005/11/03 17:16

DOCUMENT-IDENTIFIER: US 20050085090 A1

TITLE: Method for controlling accuracy and repeatability of an etch process

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Abstract Paragraph - ABTX (1):

Embodiments of the invention generally relate to a method for etching in a processing platform (e.g. a cluster tool) wherein robust pre-etch and post-etch data may be obtained in-situ. The method includes the steps of obtaining pre-etched critical dimension (CD) measurements of a feature on a **substrate,** etching the feature; **treating** the etched **substrate** to reduce and/or remove sidewall polymers deposited on the feature during etching, and obtaining post-etched CD measurements. The CD measurements may be utilized to adjust the etch process to improved the accuracy and repeatability of device fabrication.

Summary of Invention Paragraph - BSTX (10):

[0008] The present invention is a method for controlling accuracy and repeatability of an etch process. Embodiments of the invention are practiced on a processing platform (e.g. a cluster tool) wherein robust pre-etch and post-etch data may be obtained in-situ. The method includes the steps of obtaining pre-etched critical dimension (CD) measurements of a feature on a **substrate,** etching the feature; **treating** the etched **substrate** to reduce and/or remove sidewall polymers deposited on the feature during etching, and obtaining post-etched CD measurements. The CD measurements may be utilized to adjust the etch process to improved the accuracy and repeatability of device fabrication.

Detail Description Paragraph - DETX (4):

[0018] Embodiments of the invention generally relate to a method for etching in a processing platform (e.g. a cluster tool) wherein robust pre-etch and post-etch data may be obtained in-situ. The method includes the steps of obtaining pre-etched critical dimension (CD) measurements of a feature on a **substrate,** etching the feature; **treating** the etched **substrate** to reduce and/or remove sidewall polymers deposited on the feature during etching, and obtaining post-etched CD measurements. The CD measurements may be utilized to adjust the etch process to improved the accuracy and repeatability of device fabrication.

Detail Description Paragraph - DETX (19):

[0033] The trimming process may be performed using a plasma etch reactor,

e.g., a Decoupled Plasma Source (DPS) II module of the CENTURA.RTM. system. The DPS II module (discussed with reference to FIG. 3 below) uses a power source (i.e., an inductively coupled antenna) to produce a **high-density inductively coupled plasma**. To determine the endpoint of the etch process, the DPS II module may also include an endpoint detection system that monitors plasma emissions at a particular wavelength, controls the process time, or performs laser interferometery, and the like.

Claims Text - CLTX (3):

3. A method of etching a feature on a substrate in a single processing tool having an etch chamber, a post-treatment chamber and an optical measuring device suitable for obtaining a metric of a critical dimension (CD) of the etch feature, the method comprising: obtaining pre-etch CD information of the feature formed on the substrate; etching the substrate; wherein said etch process deposits a polymer on a sidewall of the feature; post-etch **treating the substrate** to reduce a thickness of the polymer disposed on the feature during etching; and obtaining post-etch CD information of the feature.

Claims Text - CLTX (4):

4. The method of claim 3, wherein the step of post-etch **treating** further comprises: exposing the **substrate** to a remotely generated plasma formed from a gas mixture of one or more of nitrogen (N.sub.2), hydrogen (H.sub.2) and oxygen (O.sub.2).

Claims Text - CLTX (6):

6. The method of claim 3, wherein the step of post-etch **treating** further comprises: maintaining a **substrate** temperature between 200 and 350 degrees Celsius.

US-PAT-NO: 6589611

DOCUMENT-IDENTIFIER: US 6589611 B1
See image for Certificate of Correction

TITLE: Deposition and chamber treatment methods

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Brief Summary Text - BSTX (16):

An exemplary prior art process for depositing material on a wafer surface and cleaning a reaction chamber is described with reference to FIG. 3. Initially, a wafer is placed within the reaction chamber. A deposit is then formed over the wafer surface, and the wafer is subsequently removed from the reaction chamber. After the **wafer** has been removed from the reaction chamber, interior sidewalls of the chamber are cleaned (typically a dry clean), and then the process can be repeated to **treat another wafer**. Accordingly, in typical prior art processes a single wafer is processed prior to cleaning internal sidewalls of a reaction chamber. It is noted that some chambers are configured to process a batch of two or more wafers. In such processes, material is deposited over the batch of wafers, and the batch is subsequently removed from the wafer prior to cleaning interior sidewalls of the chamber. In any event, typical prior art processes comprise providing a set of one or more wafers within a reaction chamber, forming a deposit over the set of wafers, and then cleaning interior sidewalls of the chamber before another set of wafers is processed.

Drawing Description Text - DRTX (9):

FIG. 7 is a flow-chart diagram describing an exemplary process of the present invention for depositing material over a **wafer** surface, and subsequently **treating** internal sidewalls of a reaction chamber.

Drawing Description Text - DRTX (10):

FIG. 8 is a flow-chart diagram of another exemplary process of the present invention for forming a deposit over a **wafer** surface and subsequently **treating** internal sidewalls of a reaction chamber.

Detailed Description Text - DETX (2):

The invention includes methods of **treating** a material (or film) along internal sidewalls of a reaction chamber to increase the number of **wafers** that

can be treated between cleanings of the internal sidewalls of the reaction chamber. As a film forms along an internal sidewall of a reaction chamber, the film eventually reaches a thickness at which it begins to peel off the chamber wall. Particles from the peeling film can fall onto a wafer within the chamber and cause various problems discussed previously in the "Background" section of this disclosure. The invention includes processes for treating a film along an internal sidewall of a reaction chamber to increase the thickness of the film that can occur before peeling begins. Since the treated film can become thicker before peeling and causing particles, more wafers can be processed than could have been processed without the treatment. The throughput of HDP-CVD processes can be limited by the frequency with which cleaning of internal sidewalls of a reaction chamber is done. Accordingly, a process that can run 1 clean for every 5 deposition wafers (typically referred to as a 5.times. clean) can have a higher throughput than one that can only run one clean for every 3 depositions (typically referred to as a 3.times. clean). Accordingly, treatment of a film deposited on an internal sidewall can increase the throughput of an HDP-CVD process.

Detailed Description Text - DETX (8):

In one exemplary method of the present invention, the material deposited over the wafer surface is silicon dioxide, and is formed by flowing silane and one or more oxygen precursors into the reaction chamber. The plasma within the reaction chamber is powered with a radio frequency power of at least 3,000 watts, and in some applications even greater than 4,000 watts. The deposition of the silicon dioxide can be accomplished by conventional processing, and accordingly the wafer can be biased relative to the plasma within conventional parameters. As a material is deposited on the wafer, a film forms on the chamber sidewalls as described previously in the "Background" section of this disclosure. After the material has been deposited on the **wafer** surface, the next step of the FIG. 7 process is to **treat** the film formed along the internal sidewalls of the chamber to enhance adhesion of the film along the sidewalls. The treatment can be accomplished by changing the conditions within the reaction chamber from deposition conditions to conditions which expose internal sidewall peripheries of the reaction chamber to activated species formed from the plasma. Such change in the conditions within the reaction chamber can include reducing a flow of one or more precursors into the chamber and/or changing the plasma from being primarily inductively coupled to being primarily capacitively coupled.

Detailed Description Text - DETX (15):

Referring to FIG. 8, the process described therein is similar to that of FIG. 7, but comprises removal of the **wafer** from within the reaction chamber

prior to **treating** the film along with the internal sidewalls of the chamber, rather than leaving the **wafer** within the chamber during the treatment of the film. The conditions utilized for treating the internal sidewalls of the chamber of the FIG. 8 process can be identical to those described above with reference to the FIG. 7 process. Also, the number of times "X" that sets of wafers are cycled through the FIG. 8 process between cleanings can be identical to that described with reference to the process of FIG. 7.

Claims Text - CLTX (30):

30. A silicon dioxide deposition method comprising: providing a substrate within a reaction chamber, the reaction chamber having an internal surface; forming a **high density plasma that is primarily inductively** coupled within the chamber; while the high density plasma is within the chamber, flowing silane and O.sub.2 into the chamber and depositing silicon dioxide onto the substrate from the silane and O.sub.2 ; a material forming on the internal surface of the chamber during the depositing of the silicon dioxide; and after depositing the silicon dioxide and while the substrate remains within the chamber; changing the plasma to a plasma that is primarily capacitively coupled; the primarily capacitively coupled plasma being utilized to alter the material on the internal surface of the chamber.

US-PAT-NO: 6515336

DOCUMENT-IDENTIFIER: US 6515336 B1

TITLE: Thin film transistors having tapered gate electrode and taped insulating film

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Brief Summary Text - BSTX (15):

The gate electrode is formed by using a heat-resistant electrically conductive material such as tungsten (W), tantalum (Ta) or titanium (Ti), or a compound of the above element, or an alloy thereof. The heat-resistant electrically conductive material is etched at a high speed and precisely forming an end in a tapered shape, relying upon a dry-etching method using a high-density plasma. A high-density plasma can be obtained by using an etching device utilizing microwaves or inductively coupled plasma (ICP). In particular, the ICP etching device easily controls the plasma and makes it possible to **treat** even those **substrates** having large areas.

Brief Summary Text - BSTX (20):

To obtain the **inductively coupled plasma of a high density,** the high-frequency current J must be supplied into the antenna coil with a low loss and, hence, the inductance must be decreased. This can be effectively done by splitting the antenna coil. FIG. 17B is a diagram illustrating the constitution thereof, wherein four spiral coils (multi-spiral coils) 910 are arranged on a quartz plate 911 and are connected to a first high-frequency power source 908 through a matching box 909. Here, if the length of each coil is set to be an integer times of one-fourth of the wavelength of the high frequency, a standing wave is formed on the coil enhancing a peak voltage that is generated.

Detailed Description Text - DETX (13):

A p-type impurity element may be added to the whole surfaces of the island-like semiconductor layers at a concentration of about 1.times.10.sup.16 to 5.times.10.sup.17 atoms/cm.sup.3 in order to control the threshold voltage (Vth) of the TFTs. The impurity elements for imparting the p-type to the semiconductor are the elements of the Group 13 of periodic table, such as boron (B), aluminum (Al) and gallium (Ga). The impurities can be added by the ion injection method or the ion doping method (or ion shower doping method). Here,

however, the ion doping method is suited for **treating the substrate** having a large area. In the ion doping method, boron (B) is added while using diborane (B.sub.2 H.sub.6) as a source gas. The impurity element needs not necessarily be injected, but is injected to confine the threshold voltage of the n-channel TFT within a predetermined range.